

VMMK-3803

3 - 11 GHz UWB Low Noise Amplifier in SMT Package



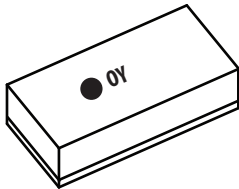
Data Sheet



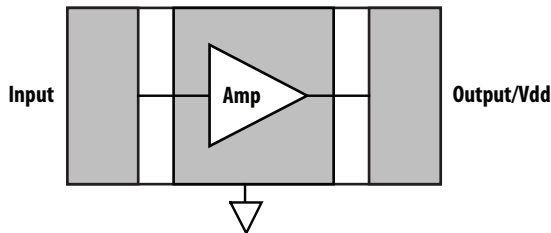
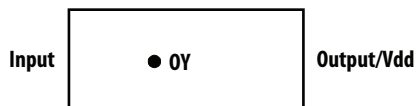
Description

The VMMK-3803 is a small and easy-to-use, broadband, low noise amplifier operating in various frequency bands from 3 to 11 GHz with typical noise figure of 1.5 dB. It is housed in the Avago Technologies' industry-leading and revolutionary sub-miniature chip scale package (GaAsCap wafer scale leadless package) which is small and ultra thin yet can be handled and placed with standard 0402 pick and place assembly equipment. The VMMK-3803 provides a typical gain of 20 dB with good linearity of 0.9 dBm typical IIP3 and input and output return losses and can be operated from 3 to 5 V power supply. It is fabricated using Avago Technologies unique 0.25 μm E-mode PHEMT technology which eliminates the need for negative gate biasing voltage.

WLP0402, 1 mm x 0.5 mm x 0.25 mm



Pin Connections (Top View)



Note:
"O" = Device Code
"Y" = Month Code

Features

- 1 x 0.5 mm surface mount package
- Ultrathin (0.25 mm)
- Wide frequency range
- Self-Biasing: 3 to 5 V
- In and output match: 50 ohm

Specifications

(6 GHz, Vdd = 3 V, Vpd = 3 V, Zin = Zout = 50 Ω)

- Low noise figure: 1.5 dB typ.
- Small signal gain: 20 dB typ.
- Output Power at 1dB compression = 7 dBm

Applications

- 3.1-10.6 GHz UWB LNA
- 3.5 and 5-6 GHz WLAN and WiMax
- 10.5 GHz PMP
- 802.16 & 802.20 BWA systems
- Radar and ECM systems
- Generic IF amplifier



Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model = 60 V
ESD Human Body Model = 200 V
Refer to Avago Application Note A004R: Electrostatic Discharge, Damage and Control.

Electrical Specifications

Table 1. Absolute Maximum Rating [1]

| Symbol | Parameters/Condition | Unit | Absolute Max |
|--------------------------|------------------------------|------|--------------|
| Vdd | Supply Voltage (RF Output) | V | 7 |
| Vpd | Power Down Voltage | V | 7 |
| Idd [2] | Supply Current | mA | 45 |
| P _{in, max} [3] | CW RF Input Power (RF Input) | dBm | 15 |
| P _{diss} | Total Power Dissipation | mW | 315 |
| T _{ch} | Max Channel Temperature | °C | +150 |
| θ _{JC} [4] | Thermal Resistance | °C/W | 90.6 |

Notes

1. Operation of this device above any one of these parameters may cause permanent damage
2. Bias is assumed DC quiescent conditions
3. With the DC (typical bias) and RF applied to the device at board temperature T_b = 25° C
4. Thermal resistance is measured from junction to board using IR method

Table 2. DC and RF Specifications [1]

T_A = 25° C, Z_{in} = Z_{out} = 50 Ω, Freq = 6 GHz, Vdd = 3 V, Vpd = 3 V (unless otherwise specified)

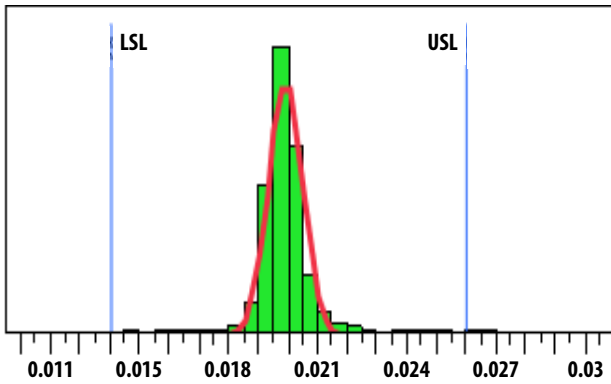
| Symbol | Parameters/Condition | Unit | Minimum | Typical | Maximum |
|-------------|---|------|---------|---------|---------|
| Idd [2] | Supply Current | mA | 14 | 20 | 26 |
| Idd_Off [2] | Leakage Current (Vpd = 0 V) | μA | | 0.1 | |
| Ga [2,3] | Gain | dB | 17 | 20 | 23 |
| NF [2,3] | Noise Figure | dB | | 1.5 | 1.9 |
| S11 [4] | Input Return Loss | dB | | 15 | |
| S22 [4] | Output Return Loss | dB | | 9 | |
| IIP3 [4,5] | Input 3 rd Order Intercept Point | dBm | | 0.9 | |
| P-1dB [4] | Output Power at 1dB Compression | dBm | | 7 | |

Notes

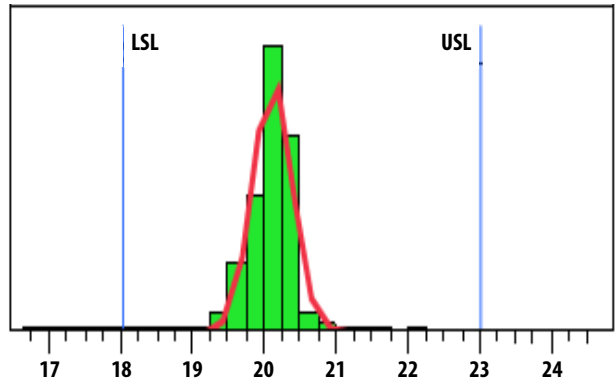
1. Losses of the test system have been de-embedded from final data
2. Measured data obtained from wafer-probing using a G-S, S-G pyramid probe
3. Ga and NF obtained from Noise Figure Analyzer
4. S-parameters, P1dB, and IIP3 data obtained using 300 μm G-S-G probing on PCB substrate
5. IIP3 test condition: Center frequency = 6 GHz, 2 tone offset = 10 MHz, Pin = -20 dBm

Product Consistency Distribution Charts at 6.0 GHz, Vdd = 3 V, Vpd = 3 V unless specified.

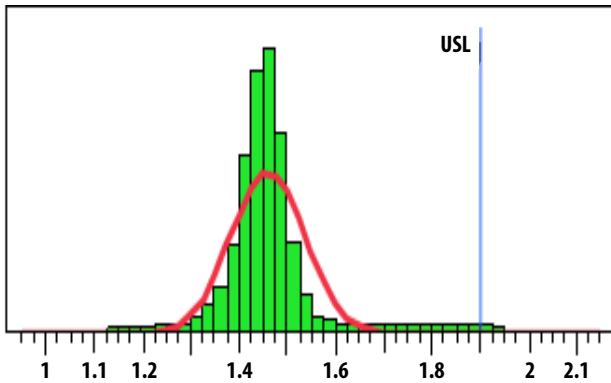
Measured data obtained from wafer-probing using a G-S, S-G pyramid probe.



Idd @ Vdd = 3 V, Vpd = 3 V, Mean = 20 mA, LSL = 14 mA, USL = 26 mA



Ga @ 6 GHz, Mean = 20 dB, LSL = 17 dB, USL = 23 dB
(Data obtained using Noise Figure Analyzer)



NF @ 6 GHz, Mean = 1.5 dB, USL = 1.9 dB

Notes:
Distribution data based on 48 Kpcs part sample size from MPV lots.
Future wafers allocated to this product may have nominal values
anywhere between the upper and lower limits.

VMMK-3803 Typical Performance

$T_A = 25^\circ\text{C}$, $V_{pd} = 3\text{ V}$, $Z_{in} = Z_{out} = 50\ \Omega$ (unless noted); data obtained using $300\ \mu\text{m}$ G-S-G probing on PCB substrate & broadband bias tees, losses calibrated out to the package reference plane.

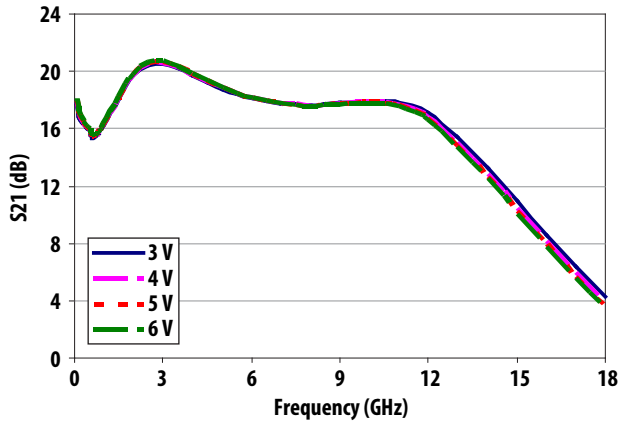


Figure 1. Small Signal Gain over Vdd

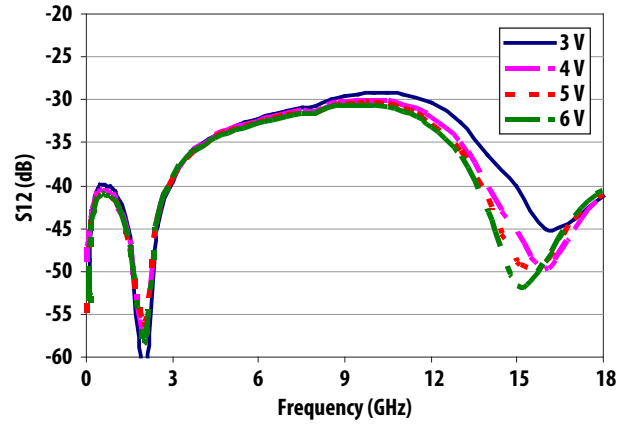


Figure 2. Reverse Isolation over Vdd

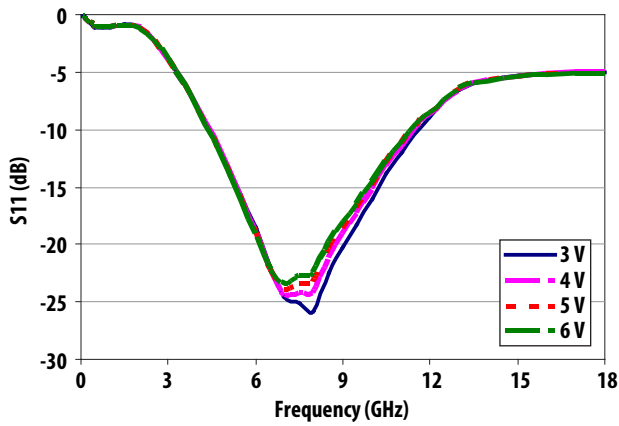


Figure 3. Input Return Loss over Vdd

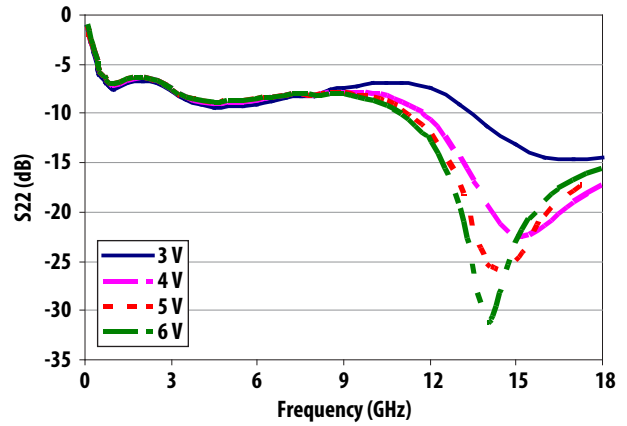


Figure 4. Output Return Loss over Vdd

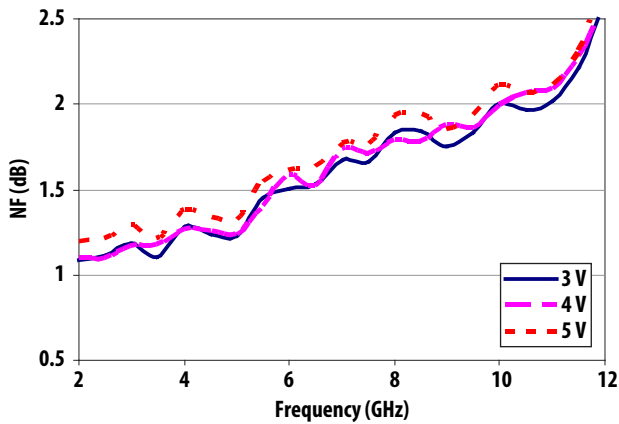


Figure 5. Noise Figure (50 ohm) over Vdd

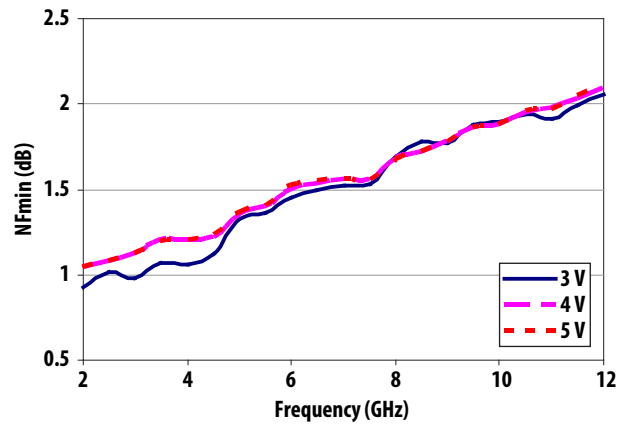


Figure 6. NFmin over Vdd

VMMK-3803 Typical Performance

$Z_{in} = Z_{out} = 50 \Omega$, $V_{pd} = 3 \text{ V}$, $T_A = 25^\circ \text{ C}$ for varying V_{dd} data, $V_{dd} = 3 \text{ V}$ for varying Temp data; obtained using $300 \mu\text{m}$ G-S-G PCB substrate & broadband bias tees, losses calibrated out to the package reference plane.

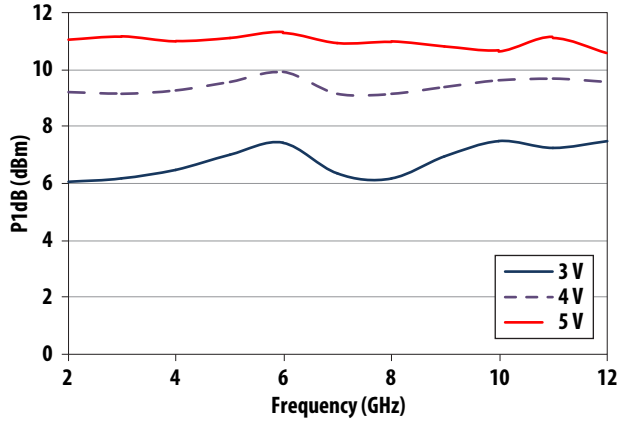


Figure 7. Output P1dB over Vdd

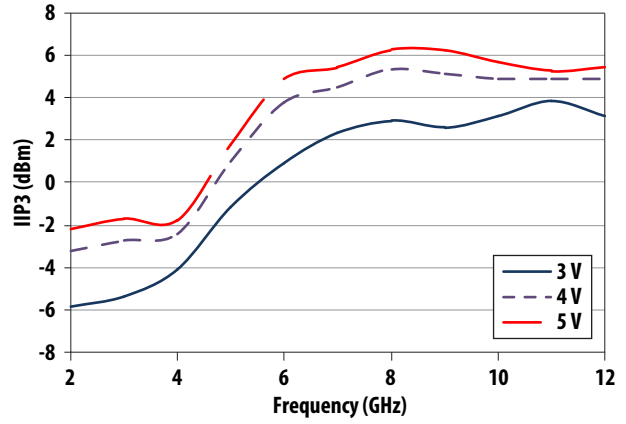


Figure 8. Input IP3 over Vdd

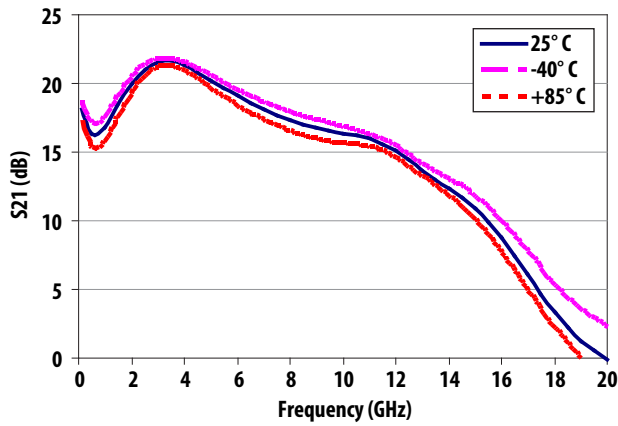


Figure 9. S21 over Temp

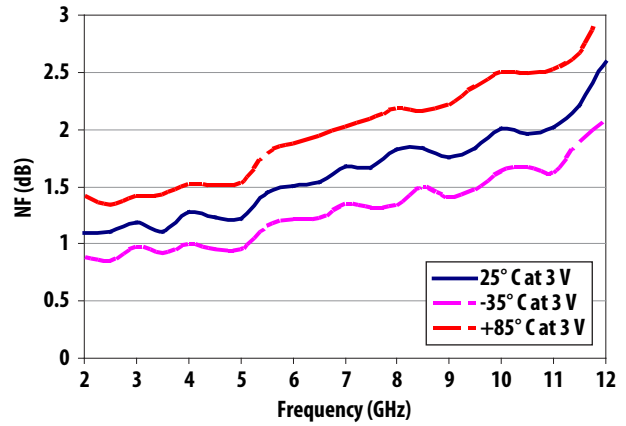


Figure 10. Noise Figure over Temp

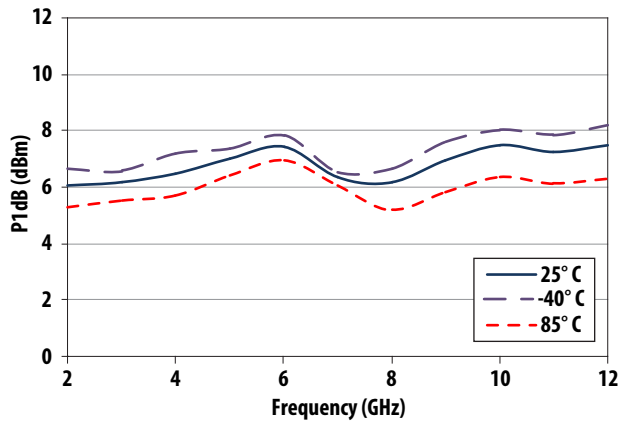


Figure 11. Output P1dB over Temp

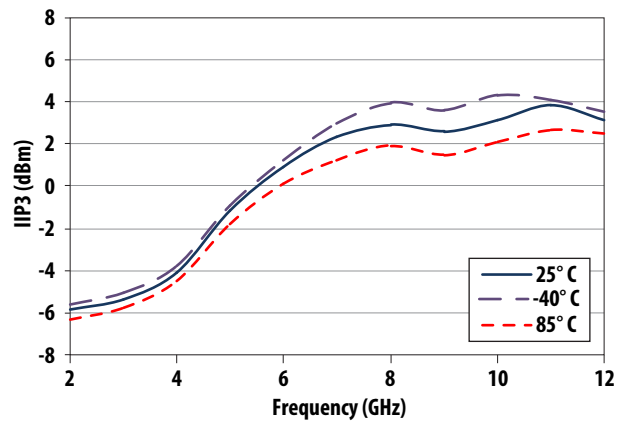


Figure 12. Input IP3 over Temp

Typical Scattering Parameters and Noise Parameters

$T_A = 25^\circ \text{C}$, $V_{dd} = 3 \text{V}$, $V_{pd} = 3 \text{V}$, $Z_{in} = Z_{out} = 50 \Omega$; data obtained using $300 \mu\text{m}$ G-S-G probing on PCB substrate & broadband bias tees, losses calibrated out to the package reference plane.

| Freq (GHz) | S11 | | | S21 | | | S12 | | | S22 | | |
|------------|--------|--------|---------|--------|---------|---------|--------|--------|---------|---------|--------|---------|
| | (dB) | (mag) | (ang) | (dB) | (mag) | (ang) | (dB) | (mag) | (ang) | (dB) | (mag) | (ang) |
| 0.5 | -1.071 | 0.884 | -17.999 | 15.88 | 6.2228 | 91.657 | -39.83 | 0.0102 | 25.085 | -5.979 | 0.5024 | -32.091 |
| 1 | -1.068 | 0.8843 | -28.599 | 16.228 | 6.4776 | 54.832 | -40.72 | 0.0092 | -5.7032 | -7.5392 | 0.4198 | -21.41 |
| 2 | -1.151 | 0.8759 | -64.841 | 19.703 | 9.6641 | -0.2142 | -61.94 | 0.0008 | 26.203 | -6.6846 | 0.4632 | -30.788 |
| 2.5 | -2.194 | 0.7768 | -82.84 | 20.424 | 10.5006 | -26.683 | -44.73 | 0.0058 | 94.308 | -6.9512 | 0.4492 | -42.359 |
| 3 | -3.833 | 0.6432 | -100.89 | 20.494 | 10.5852 | -50.965 | -39.49 | 0.0106 | 80.488 | -7.8145 | 0.4067 | -50.364 |
| 3.5 | -5.869 | 0.5088 | -116.6 | 20.166 | 10.1931 | -72.011 | -36.71 | 0.0146 | 67.726 | -8.6172 | 0.3708 | -54.537 |
| 4 | -8.099 | 0.3936 | -129.96 | 19.68 | 9.6383 | -90.299 | -35.19 | 0.0174 | 57.244 | -9.1311 | 0.3495 | -57.475 |
| 4.5 | -10.46 | 0.3 | -141.47 | 19.205 | 9.1254 | -106.48 | -34.11 | 0.0197 | 48.809 | -9.35 | 0.3408 | -60.009 |
| 5 | -12.98 | 0.2243 | -150.4 | 18.755 | 8.6649 | -121.1 | -33.43 | 0.0213 | 41.646 | -9.231 | 0.3455 | -62.991 |
| 5.5 | -15.61 | 0.1658 | -160.11 | 18.399 | 8.317 | -135.11 | -32.69 | 0.0232 | 37.431 | -9.231 | 0.3455 | -67.759 |
| 6 | -18.59 | 0.1176 | -166.04 | 18.111 | 8.0454 | -148.18 | -32.22 | 0.0245 | 31.778 | -9.0199 | 0.354 | -72.539 |
| 6.5 | -21.86 | 0.0807 | -167.23 | 17.923 | 7.8735 | -160.97 | -31.67 | 0.0261 | 26.223 | -8.7328 | 0.3659 | -78.294 |
| 7 | -24.5 | 0.0596 | -160.39 | 17.775 | 7.7401 | -173.68 | -31.24 | 0.0274 | 20.235 | -8.4272 | 0.379 | -85.286 |
| 7.5 | -25.11 | 0.0555 | -149.66 | 17.709 | 7.6816 | 173.48 | -30.84 | 0.0287 | 14.279 | -8.1787 | 0.39 | -93.407 |
| 8 | -25.75 | 0.0516 | -142.86 | 17.606 | 7.5906 | 160.8 | -30.75 | 0.029 | 11.758 | -8.1809 | 0.3899 | -100.46 |
| 8.5 | -22.45 | 0.0754 | -140.76 | 17.709 | 7.6817 | 147.9 | -29.95 | 0.0318 | 3.8768 | -7.6181 | 0.416 | -109.34 |
| 9 | -20.23 | 0.0974 | -152.95 | 17.786 | 7.7502 | 134.22 | -29.58 | 0.0332 | -3.334 | -7.3711 | 0.428 | -119.64 |
| 9.5 | -18.22 | 0.1228 | -169.1 | 17.843 | 7.8006 | 120.1 | -29.34 | 0.0341 | -11.824 | -7.1844 | 0.4373 | -130.1 |
| 10 | -16 | 0.1584 | 174.25 | 17.902 | 7.8542 | 105.21 | -29.24 | 0.0345 | -20.194 | -6.9803 | 0.4477 | -141.68 |
| 10.5 | -13.79 | 0.2043 | 156.38 | 17.934 | 7.8828 | 89.54 | -29.12 | 0.035 | -29.569 | -6.8455 | 0.4547 | -154.5 |
| 11 | -11.97 | 0.2521 | 137.68 | 17.788 | 7.7516 | 73.292 | -29.37 | 0.034 | -40.032 | -6.9454 | 0.4495 | -167.89 |
| 12 | -8.92 | 0.3581 | 100.89 | 17.121 | 7.179 | 38.405 | -30.31 | 0.0305 | -63.682 | -7.4568 | 0.4238 | 162.538 |
| 13 | -6.614 | 0.467 | 65.61 | 15.39 | 5.8818 | 3.9724 | -32.58 | 0.0235 | -89.863 | -9.1485 | 0.3488 | 127.677 |
| 14 | -5.764 | 0.515 | 38.532 | 13.256 | 4.6006 | -25.269 | -36.42 | 0.0151 | -115.26 | -11.258 | 0.2736 | 97.5178 |
| 15 | -5.333 | 0.5412 | 17.245 | 10.905 | 3.5095 | -50.943 | -40.09 | 0.0099 | -141.77 | -13.159 | 0.2198 | 70.0208 |
| 16 | -5.106 | 0.5555 | -0.6043 | 8.5552 | 2.6777 | -73.397 | -45.04 | 0.0056 | 163.4 | -14.462 | 0.1892 | 42.6539 |
| 17 | -5.002 | 0.5622 | -15.312 | 6.3253 | 2.0714 | -93.815 | -43.88 | 0.0064 | 123.41 | -14.699 | 0.1841 | 17.9161 |
| 18 | -5.002 | 0.5622 | -28.024 | 4.239 | 1.6291 | -112.86 | -41.31 | 0.0086 | 86.597 | -14.485 | 0.1887 | -3.435 |

| Freq (GHz) | Fmin (dB) | Rn | Γ_{opt} (mag) | Γ_{opt} (ang) | Associated gain (dB) |
|------------|-----------|-------|----------------------|----------------------|----------------------|
| 2 | 0.93 | 0.279 | 0.504 | 35.48 | 23.81 |
| 2.5 | 1.02 | 0.241 | 0.440 | 41.07 | 22.90 |
| 3 | 0.98 | 0.168 | 0.574 | 33.56 | 20.48 |
| 4 | 1.06 | 0.169 | 0.378 | 54.74 | 20.17 |
| 5 | 1.33 | 0.152 | 0.304 | 80.24 | 19.46 |
| 5.5 | 1.36 | 0.156 | 0.306 | 86.48 | 19.07 |
| 6 | 1.45 | 0.142 | 0.234 | 88.16 | 18.92 |
| 7 | 1.52 | 0.120 | 0.141 | 126.58 | 18.80 |
| 8 | 1.69 | 0.120 | 0.143 | 126.9 | 18.88 |
| 9 | 1.77 | 0.117 | 0.108 | 152.56 | 19.22 |
| 10 | 1.93 | 0.122 | 0.111 | -161.83 | 19.38 |
| 10.5 | 1.94 | 0.162 | 0.113 | -141.3 | 19.50 |
| 11 | 1.91 | 0.142 | 0.113 | -151.1 | 19.17 |
| 12 | 2.06 | 0.220 | 0.082 | -61.09 | 18.16 |
| 13 | 2.4 | 0.260 | 0.165 | -58.95 | 16.77 |

VMMK-3803 Applications Information

Biasing and Operation

The VMMK-3803 is biased with a positive supply connected to the output pin Vd through an external user supplied bias decoupling network. Typical bias is 3 V at 20 mA. The “on” state also requires that the input port of the VMMK-3803 also be biased at 3 V for normal gain operation. 0V on the input puts the VMMK-3803 in the “off” state.

An example of simple user supplied bias tees is shown in Figure 13. The output bias decoupling network feeding Vdd consists of a shunt 6.8 nH inductor. At the input, a 10 Kohm resistor is needed to feed the power-down control voltage. The input and output dc blocking capacitors are each 100 pF. The “on” and “off” S Parameters shown in the preceding tables reflect the operation of the circuit shown in Figure 14.

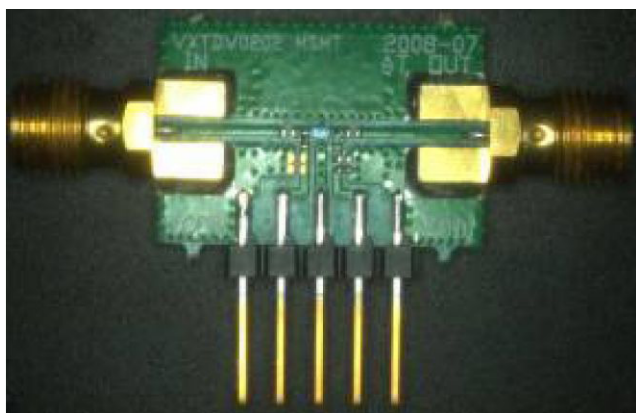


Figure 13. Demo Board (available to qualified customers upon request)

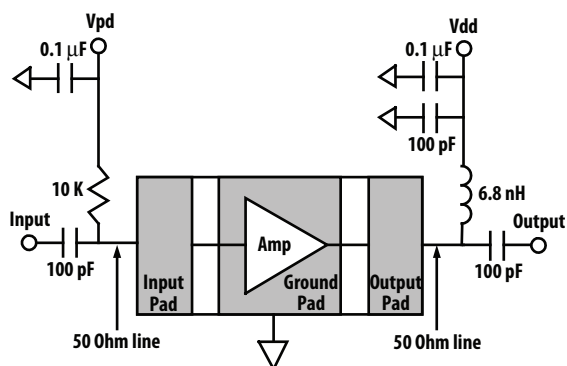


Figure 14. Example demonstration circuit of VMMK-3803 for broadband operation (3GHz to 11GHz).

A layout of a typical demo board is shown in Figure 15.

Table 3. VMMK-3803 Demo Board BOM

| Component | Value |
|-----------|-----------|
| DUT | VMMK-3803 |
| C1 | 100 pF |
| C2 | 100 pF |
| R1 | 10 kohm |
| C5 | 0.1 μF |
| C6 | 100 pF |
| L1 | 6.8 nH |

The input and output bias decoupling network can be easily constructed using small surface mount components. The value of the shunt inductors can have a major effect on both low and high frequency operation. The demo board uses small value inductors that have self resonant frequencies higher than the maximum desired frequency of operation. If the self-resonant frequency of the inductor is too close to the operating band, the value of the inductor will need to be adjusted so that the self-resonant frequency is significantly higher than the highest frequency of operation.

Typically a passive component company like Murata does not specify S parameters at frequencies higher than 5 or 6 GHz for larger values of inductance making it difficult to properly simulate amplifier performance at higher frequencies. It has been observed that the Murata LQW15AN series of 0402 inductors actually works quite well above their normally specified frequency.

The parallel combination of the 100 pF and 0.1 μF bypass capacitors provide a low impedance in the band of operation and at lower frequencies and should be placed as close as possible to the inductor. The low frequency bypass provides good rejection of power supply noise and also provides a low impedance termination for third order low frequency mixing products that will be generated when multiple in-band signals are injected into any amplifier.

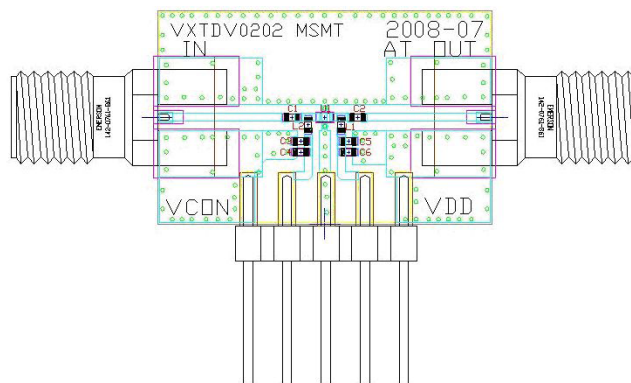


Figure 15. Biasing the VMMK-3803

S Parameter Measurements

The S-parameters are measured on a 0.016 inch thick RO4003 printed circuit test board, using G-S-G (ground signal ground) probes. Coplanar waveguide is used to provide a smooth transition from the probes to the device under test. The presence of the ground plane on top of the test board results in excellent grounding at the device under test. A combination of SOLT (Short – Open – Load – Thru) and TRL (Thru – Reflect – Line) calibration techniques are used to correct for the effects of the test board, resulting in accurate device S parameters.

Package and Assembly Note

For detailed description of the device package, handling and assembly, refer to Application Note 5378.

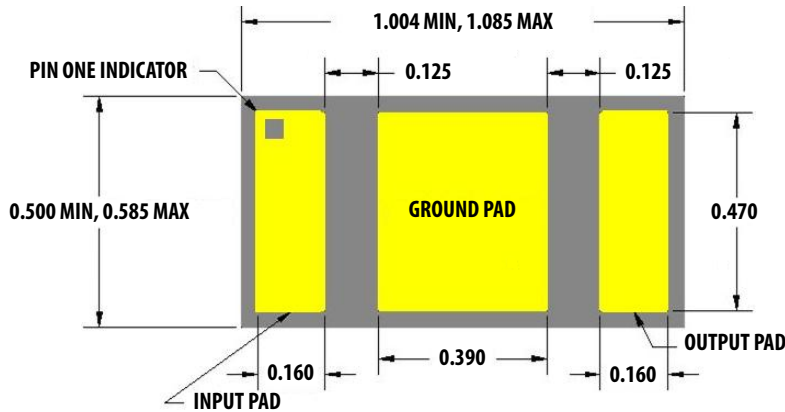
ESD Precautions

Note: These devices are ESD sensitive. The following precautions are strongly recommended. Ensure that an ESD approved carrier is used when die are transported from one destination to another. Personal grounding is to be worn at all times when handling these devices. For more detail, refer to Avago application note *A004R: Electro-static Discharge Damage and Control*.

Ordering Information

| Part Number | Devices Per Container | Container |
|--------------------|------------------------------|------------------|
| VMMK-3803-BLKG | 100 | Antistatic Bag |
| VMMK-3803-TR1G | 5000 | 7" Reel |

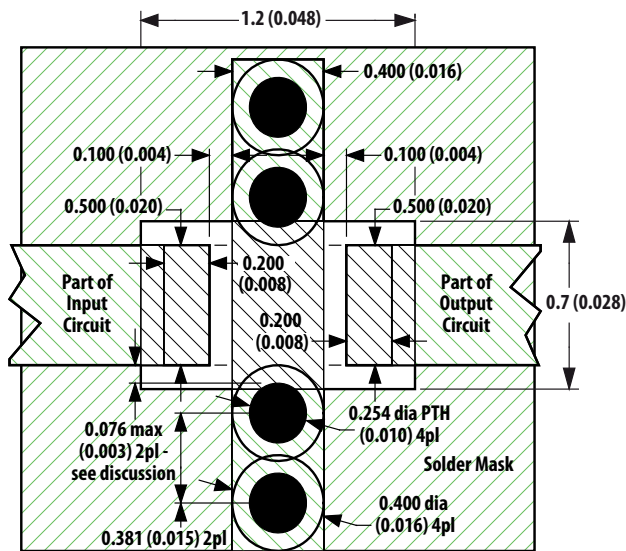
Outline Drawing



Notes:

Solderable area of the device shown in yellow.
 Dimensions in mm.
 Tolerance ± 0.015 mm

Suggested PCB Material and Land Pattern



Notes:

- 0.010" Rogers RO4350

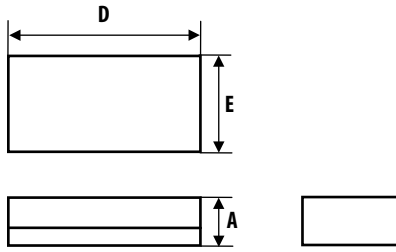
Recommended SMT Attachment

The VMMK Packaged Devices are compatible with high volume surface mount PCB assembly processes.

Manual Assembly for Prototypes

- Follow ESD precautions while handling packages.
- Handling should be along the edges with tweezers or from topside if using a vacuum collet.
- Recommended attachment is solder paste. Please see recommended solder reflow profile. Conductive epoxy is not recommended. Hand soldering is not recommended.
- Apply solder paste using either a stencil printer or dot placement. The volume of solder paste will be dependent on PCB and component layout and should be controlled to ensure consistent mechanical and electrical performance. **Excessive solder will degrade RF performance.**
- Follow solder paste and vendor's recommendations when developing a solder reflow profile. A standard profile will have a steady ramp up from room temperature to the pre-heat temp to avoid damage due to thermal shock.
- Packages have been qualified to withstand a peak temperature of 260°C for 20 to 40 sec. Verify that the profile will not expose device beyond these limits.
- Clean off flux per vendor's recommendations.
- Clean the module with Acetone. Rinse with alcohol. Allow the module to dry before testing.

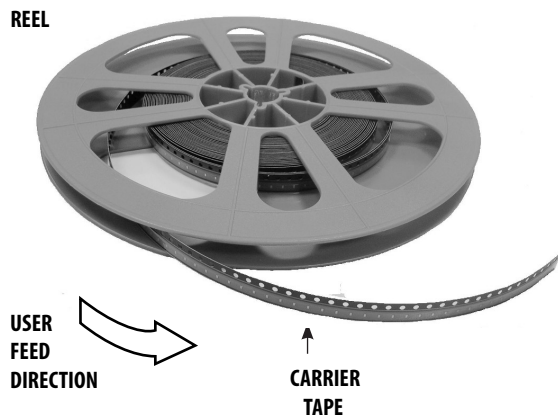
Package Dimension Outline



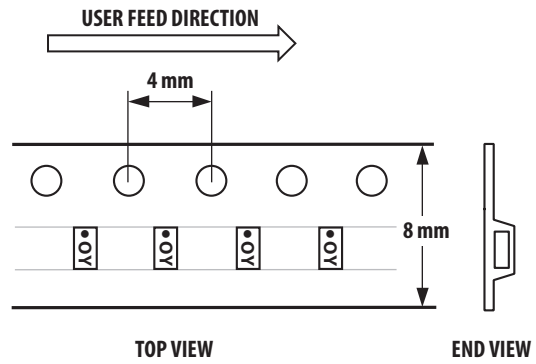
| Dimensions Symbol | Min (mm) | Max (mm) |
|-------------------|----------|----------|
| E | 0.500 | 0.585 |
| D | 1.004 | 1.085 |
| A | 0.225 | 0.275 |

Note:
All dimensions are in mm

Reel Orientation

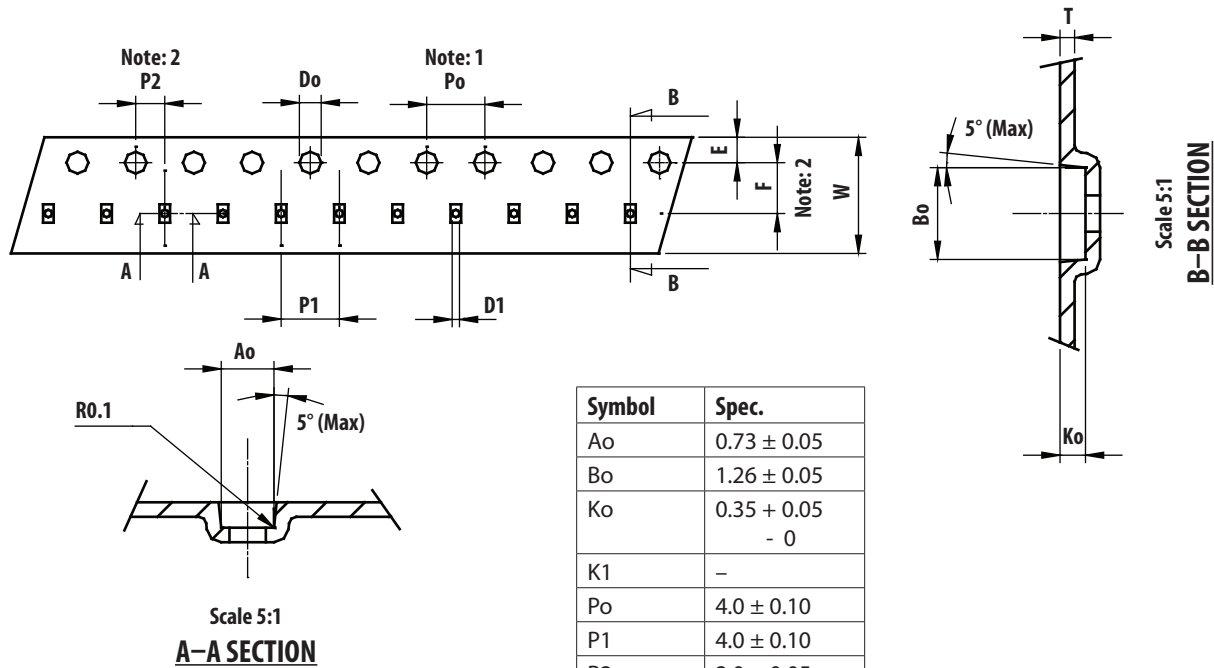


Device Orientation



Notes:
"O" = Device Code
"Y" = Month Code

Tape Dimensions



Unit: mm

Notes:

1. 10 Sprocket hole pitch cumulative tolerance is ± 0.1 mm.
2. Pocket position relative to sprocket hole measured as true position of pocket not pocket hole.
3. Ao & Bo measured on a plane 0.3 mm above the bottom of the pocket to top surface of the carrier.
4. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
5. Carrier camber shall be not than 1 m per 100 mm through a length of 250 mm.

For product information and a complete list of distributors, please go to our web site: www.avagotech.com

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AVAGO
TECHNOLOGIES